R09

Code No: C3801, C0602, C7001, C5508, C7706, C4505, C6806, C5706

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I - Semester Examinations, March/April 2011

DIGITAL SYSTEM DESIGN

(COMMON TO DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS, DIGITAL SYSTEMS AND COMPUTER ELECTRONICS, ELECTRONICS AND COMMUNICATION, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS AND VLSI DESIGN, SYSTEMS AND SIGNAL PROCESSING, VLSI AND EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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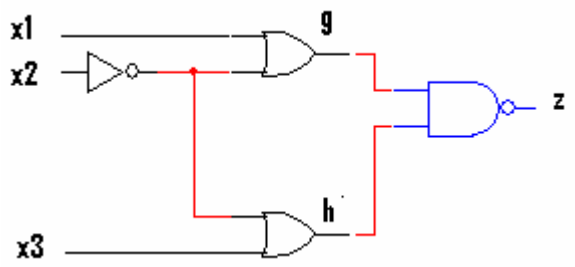
1. a) Explain design of binary divider.
   b) Explain design of parallel multiplier. [12]

2. a) Implement the following Boolean function by Hazard free OR-AND network
   $F=\sum(0,2,6,7)$.
   b) Explain signature analysis with example. [12]

3. Minimize the following function by the IISc algorithm.
   F=1100 + 1211 + 0110 + 0001 + 2121. [12]

4. a) Derive by the path sensitization method the test vectors for SA-0 and SA-1 faults at g and h in the network.



   b) Find the test vectors of all SA0 and SA1 faults of the circuit function. [12]
   $F= x_1x_2+x_1x_3'x_4'+x_2x_4$ using Kohavi algorithm.

Contd…..2

5.

PS	NS	
	X=0	X=1
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

Implement the following using above machine
a) Homing tree.
b) Synchronizing tree.

6. Write short notes for the following:
   a) D algorithm
   b) PODEM

7. a) Explain bridge fault model.
   b) Design a decade counter using T Flip Flop and OR- AND gates.

8. Design a Mealy sequential circuit which investigates an input sequence X and will produce an output Z=1 for any input sequence ending in 0010 or 100
   X=110010010100101
   Z=000101101001010

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